Efficient Design Space Exploration for Chip Multiprocessors

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ABSTRACT

Increases in architectural design space for CMP’s motivate efficient, scalable simulation and modeling frameworks.

- We summarize our recent experiences in CMP simulation.
  - pipeline analysis
  - thermal analysis

- Observations from prior work motivate future work.
  - statistical significance ranking
  - regression modeling

EXPERIENCE Pipeline Depth/ Width Analysis

“Effects of Pipeline Complexity on SMT/ CMP Power-Performance Efficiency” (WCEI’05)

- Methodology
  - Metrics: Performance, Power
  - Parameters: Pipeline dimensions, threads per core (SMT), cores per chip (CMP)
  - Framework: Integrated multi-core simulation based on tracking cache conflicts between threads of throughput computing applications

- Conclusions
  - Common optimal pipeline depth/ width for ST, SMT, CMP
  - SMT, CMP enable power-performance efficient increases in core size

CONTINUING & FUTURE WORK

- Plackett-Burman
  - Designing “optimum multifactorial experiments”
  - Obtain 2N configurations varying N-1 parameters
    1. Generate a design matrix where -1, +1 assigns a lower, upper bound value to a parameter. Matrices are derived in Plackett, Burman’s paper.
    2. Simulate 2N configurations from design matrix
    3. Determine effects of parameter k (Ec = R T x Pk)
  - Objective: Identify statistically significant parameters by rank ordering them by effect | Ec |

- Regression Modeling
  - Obtain exhaustive single-core simulations varying significant design parameters
  - Derive regression models to capture design trade-offs of single core
  - Employ models to explore larger CMP design space without costs of per-core simulations
  - Objective: Scalable, efficient multi-core simulation

PROBLEM CONTEXT

- Challenges
  - Increasing number of tunable architectural parameters
    - Core complexity, Number of cores, Heterogeneous cores, Interconnect.

- Goals
  - Leverage knowledge of uni-processor, single-core design space
  - Replace per-core part of CMP simulation with regression/analytical models.
  - Evaluate for relative accuracy, ability to capture design trade-offs

EXPERIENCE Thermal Analyses

“CMP Design Space Exploration Subject to Physical Constraints” (HPCA’06), in collaboration with the University of Virginia (Yingmin Li, Kevin Skadron) and IBM (Zhigang Hu)

- Methodology
  - Metrics: Performance, Power, Thermal Efficiency, Area
  - Parameters: Pipeline dimensions, cache size, voltage/ frequency, thermal packaging
  - Framework: Decoupled core and interconnect/ cache simulation.
  - Single-core simulations provide access traces to cache simulator that penalizes performance for conflicts

- Conclusions
  - Thermal constraints dominate other constraints
  - Optimal pipeline dimensions decrease to meet thermal constraints
  - Power density increases with depth; dissipation increases faster than area.

Pipe Depth/Width Analysis

- Figure 1: Pipeline Depth

- Figure 2: Pipeline Width

- Figure 3: Before & After Thermal Constraints

Statistical Significance Ranking, Regression Modeling

- Figure 4: PB Design Matrix