ECE/CS 250 – Prof. Bletsch
Recitation #8
Pipelining

Objective: In this recitation, you will learn about real chips and improve your understanding of how ware runs on pipelines.

There are three tasks in this recitation. The UTAs will help to manage the time.

1. Pipelining, Dependences, and Hazards

Assume the 5-stage pipeline from class (and the textbook), and assume full bypassing wherever possible. Construct a 4-line MIPS code snippet with two data dependences through registers. One of the dependences should be a hazard (i.e., require a stall) and the other should not (i.e., can be resolved via bypassing).

2. Stalls and Bypasses

Assume the 5-stage pipeline we've used in class (F, D, X, M, W). Assume the pipeline forwards/bypasses operands whenever possible and stalls only when needed to satisfy a RAW dependence that can't be forwarded/bypassed. Assume all loads and stores hit in the 1-cycle data cache.

Complete a pipeline diagram for the first 7 cycles, and assume that the add is in the Fetch (F) stage in cycle 1, as shown below.

	1	**2**	**3**	**4**	**5**	**6**	**7**
add $1, $2, $3	F						
xor $2, $1, $2							
lw $1, 4($2)							
sub $2, $5, $1							
sw $2, 4($5)							

ALL DONE?

Nice! Don't head out, though. Work on the current homework and talk to the TAs for help. If you're good on the homework, start the next recitation, which is exploratory and open-ended.